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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/606,175	06/25/2003	Naoto Hirota	KANEKO.007AUS	1486
7590	02/09/2006		EXAMINER	
MURAMATSU & ASSOCIATES			MCPHERSON, JOHN A	
Suite 310				
114 Pacifica			ART UNIT	
Irvine, CA 92618			PAPER NUMBER	
			1756	

DATE MAILED: 02/09/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

10/606,175

Applicant(s)

HIROTA, NAOTO

Examiner

John A. McPherson

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1756

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 17 October 2005.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-4, 16 and 17 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☒ Claim(s) 1-4 is/are allowed.
- 6) ☒ Claim(s) 16 and 17 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 25 June 2003 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☒ None of:
- 1) ☒ Certified copies of the priority documents have been received.
 - 2) ☐ Certified copies of the priority documents have been received in Application No. _____.
 - 3) ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|---|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date <u>6/03, 9/05</u> | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Election/Restrictions

1. Applicant's election without traverse of Group I, claim 1-4, 16 and 17 in the reply filed on 10/17/05 is acknowledged.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the first paragraph of 35 U.S.C. 112:

The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

Claims 16 and 17 are rejected under 35 U.S.C. 112, first paragraph, as based on a disclosure which is not enabling. The presently claimed methods, which are described as requiring limitations critical or essential to the practice of the invention, but not included in the claim(s), are not enabled by the disclosure. See *In re Mayhew*, 527 F.2d 1229, 188 USPQ 356 (CCPA 1976).

Claims 16 does not include the limitations that the second photomasking step is a halftone exposing step, and that in the second photomasking step a positive resist portion having a thickness smaller than the positive resist portion corresponding to the thin-film transistor elements is formed on the other portions of the substrate. The disclosure describes these limitations as critical and essential to the practice of the invention (e.g. see page 23, line 27 to page 24, line 11 of the specification).

Similarly, claim 17 does not include the limitations that the second photomasking step is a halftone exposing step, and that in the second photomasking step a positive

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resist portion having a thickness smaller than the positive resist portion corresponding to the thin-film transistor elements is formed on the other portions of the substrate. The disclosure describes these limitations as critical and essential to the practice of the invention (e.g. see page 29, line 15 to page 30, line 3 of the specification).

3. The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 16 and 17 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claims 16 and 17 each recite the limitation "said thin-film semiconductor elements" in line 24. There is insufficient antecedent basis for this limitation in the claim. This rejection could be overcome by amending "semiconductor" to --transistor-- in line 24 of both claim 16 and 17.

Pertinent Prior Art

4. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

US 6,744,486 discloses a method of fabricating a liquid crystal device comprising the steps of forming a photoresist layer on a passivation layer; exposing the photoresist using a mask having a light shielding portion, a light transmissive portion, and semi-

transmissive portion; and forming a first photoresist portion, a second photoresist portion, and a third photoresist portion.

US 2002/0028411 discloses a method of manufacturing a thin film transistor array panel for a liquid crystal display comprising the steps of coating a positive photoresist on a passivation layer; exposing the photoresist layer to light through one or more masks having different transmittance between a display area and a peripheral area; developing the photoresist to form a photoresist pattern having a thickness that varies depending on the position, wherein a thin portion and a thick portion of the photoresist pattern are provided for the display area, and a thick portion and a zero thickness portion are provided for the peripheral area.

US 6,225,130 discloses a method for manufacturing a liquid crystal display, comprising the steps of forming a gate wire, a gate insulating layer, a semiconductor layer, and an ohmic contact layer on a substrate; coating a photoresist layer thereon; exposing the photoresist layer through a mask and developing to form a photoresist pattern, wherein a first portion of the photoresist pattern located between a source electrode and a drain electrode is thinner than a second portion which is located on the data wire, and the rest of the photoresist layer is wholly removed.

US 6,451,635 discloses a method of fabricating a thin film transistor array substrate for a liquid crystal display comprising the steps of forming a gate line assembly on a substrate; laying a plurality of layers on the substrate; depositing a photoresist film on the layers; and first exposing the photoresist at a first light exposing

unit and secondly exposing the photoresist at a second light exposing unit such that the photoresist film has three portions of different thickness.

US 6,876,428 discloses a method of manufacturing a liquid crystal display panel comprising the steps of providing a thin film; depositing a photo-sensitive layer on the thin film; exposing the photo-sensitive layer using a mask having a transparent portion and a partial transparent portion, wherein the partial transparent portion includes at least two portions having different transparent ratios; and etching the thin film using the patterned photo-sensitive layer.

Allowable Subject Matter

5. Claims 1-4 are allowed because in a process of manufacturing a liquid crystal display as set forth in claim 1 of the present invention, the prior art does not teach or suggest the process wherein the halftone exposure step forms resist-free areas on the portions of the semiconductor layer which correspond to the connecting portions as set forth in (ii).

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to John A. McPherson whose telephone number is (571) 272-1386. The examiner can normally be reached on Monday through Friday, 8:00 AM to 4:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mark Huff can be reached on (571) 272-1385. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



John A. McPherson
Primary Examiner
Art Unit 1756

JAM
2/6/06